400G QSFP-DD Breakout to 4xSFP-DD Direct Attached Cable

Features

- QSFP-DD Module compliant to QSFP-DD MSA
- SFP-DD Module compliant to SFP-DD MSA
- Transmission data rate up to 53. 125Gbps per channel
- Enable 400Gb/s to 4x100Gb/s Transmission
- Link length up to 3m
- Built-in EEPROM functions
- Operating case temperature 0°C to +70°C
- RoHS2.0 compliant

Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3. 13	3.3	3.47	V
Storage temperature	Ts	-40		85	ºC
Operating Case temperature	Tc	0		70	ºC

Humidity	Rh	5		85	%
Data Rate			400		Gbps

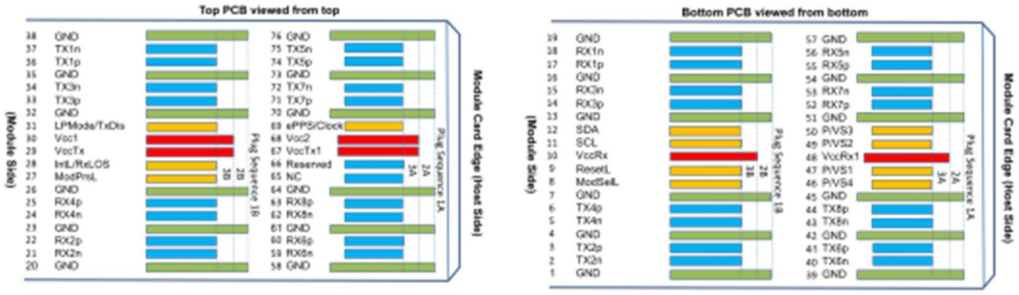
Physical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Length	L	0.5		3.0	M
AWG		30		27	AWG
Jacket material		PVC, Black (or Customization)			

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Resistance	Rcon			3	ohm
Insulation Resistance	Rins			10	Mohm
Raw cable impedance	Zca	95	100	110	ohm
Mated connector Impedance	Zmated	85	100	110	ohm
Insertion loss at 12.89 GHz	SDD21	8		17.16	dB
Return loss	SDD11/22	$Return\_loss(f)\geq \begin{cases} 16.5-2\sqrt{f} & 0.05\leq f<4.1 \\ 10.66-14\log_{10}(f/5.5) & 4.1\leq f\leq 19 \end{cases}$			dB
Differential to common-mode return loss	SCD11/22	$Return\_loss(f)\geqslant \begin{cases} 22-(20/25.78)f & 0.01\leqslant f<12.89 \\ 15-(6/25.78)f & 12.89\leqslant f\leqslant 19 \end{cases}$			dB
Differential to common-mode conversion loss	SCD21-SDD21	$Conversion\_loss(f) - IL(f)\geqslant \begin{cases} 10 & 0.01\leqslant f<12.89 \\ 27-(29/22)f & 12.89\leqslant f<15.7 \\ 6.3 & 15.7\leqslant f\leqslant 19 \end{cases}$			dB
Minimum COM	COM	3			dB

Pin Description



Electrical Pin-out Details for QSFP-DD

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	TWI serial interface clock	3B	
12	LVCMOS-I/O	SDA	TWI serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode/ TxDis	Low Power mode/optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
46	LVCMOS /CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A	5
47	LVCMOS /CML-I	P/VS1	Programmable/Module Vendor Specific 1	3A	5
48		VccRx1	3.3V Power Supply	2A	2
49	LVCMOS /CML-O	P/VS2	Programmable/Module Vendor Specific 2	3A	5
50	LVCMOS /CML-O	P/VS3	Programmable/Module Vendor Specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A	6
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a maximum current of 500 mA.

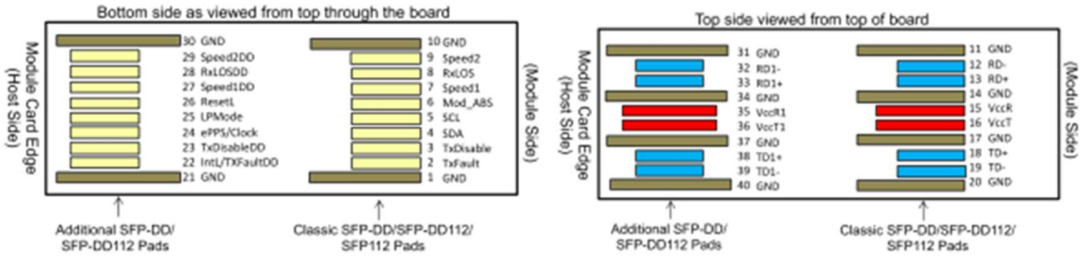
Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 10. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a maximum current of 1500 mA.

Note 3: Reserved and no Connect pads recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

Note 5: Full definitions of the P/VSx signals currently under development. On new designs not used P/VSx signals are recommended to be terminated on the host with 10 kΩ.

Note 6: ePPS/Clock if not used recommended to be terminated with 50 Ω to ground on the host.



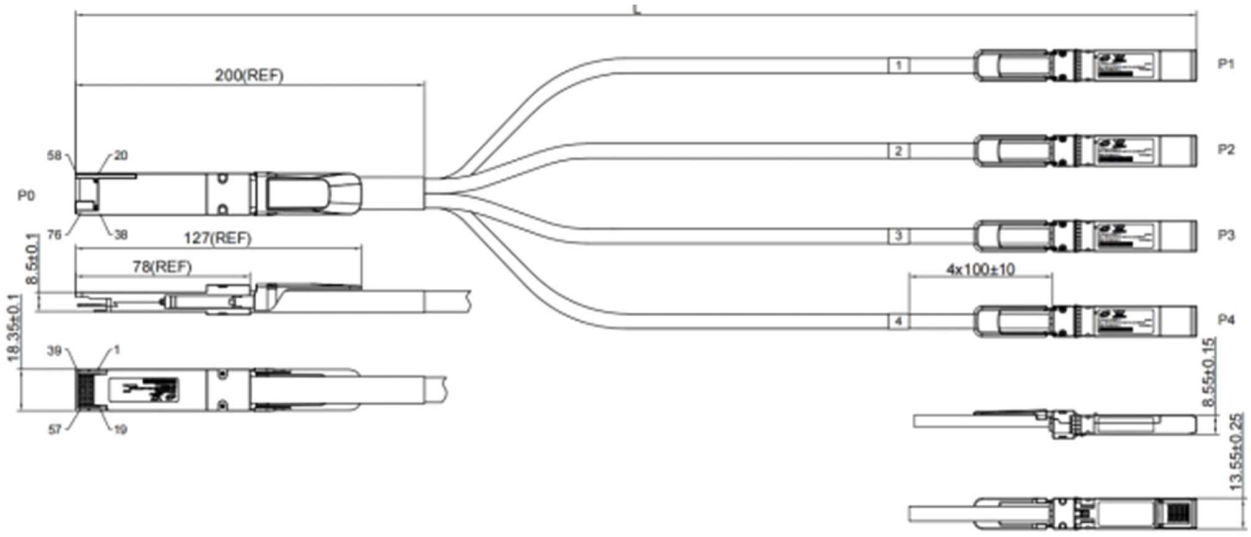
Electrical Pin-out Details for SFP-DD

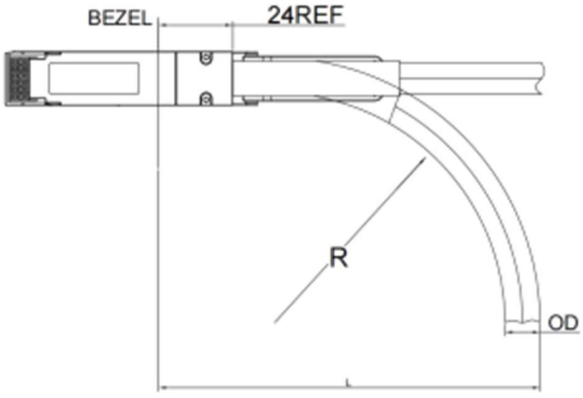
Pad	Logic	Symbol	Module Pad Descriptions	Plug Sequence[4]	Notes
0		Case	Module case	0	
1		GND	Ground	1B	1
2	LVTTL-O	TxFault	Module Fault Indication: optionally configured as classic SFP Module Fault Indication via TWI as described in the SFP-DD MIS	3B	
3	LVTTL-I	TxDisable	Transmitter Disable for classic SFP channel	3B	
4	LVCMOS-I/O	SDA	Management I/F data line	3B	
5	LVCMOS-I/O	SCL	Management I/F clock	3B	
6	LVTTL-O	Mod_ABS	Module Absent	3B	
7	LVTTL-I	Speed1	Rx Rate Select for classic SFP channel	3B	
8	LVTTL-O	RxLOS	Rx Loss of Signal for classic SFP channel	3B	
9	LVTTL-I	Speed2	Tx Rate Select for classic SFP channel	3B	
10		GND	Ground	1B	1
11		GND	Ground	1B	1
12	CML-O	RD0-	Inverse Received Data Out for classic SFP+ channel	3B	
13	CML-O	RD0+	Received Data Out for classic SFP+ channel	3B	
14		GND	Ground	1B	1
15		VccR	Receiver Power	2B	2
16		VccT	Transmitter Power	2B	2
17		GND	Ground	1B	1
18	CML-I	TD0+	Transmit Data In for classic SFP channel	3B	
19	CML-I	TD0-	Inverse Transmit Data In for classic SFP channel	3B	
20		GND	Ground	1B	1
21		GND	Ground	1A	1
22	LVTTL-O	IntL/ TxFaultDD	Interrupt: optionally configured as TxFaultDD via TWI as described in the SFP-DD MIS	3A	
23	LVTTL-I	TxDisableDD	Transmitter Disable for DD channel	3A	
24	LVTTL-I	ePPS/Clock	Precision Time Protocol (PTP) reference clock input	3A	3
25	LVTTL-I	LPMode	Low Power Mode Control	3A	
26	LVTTL-I	ResetL	Module Reset	3A	
27	LVTTL-I	Speed1DD	Rx Rate Select for DD channel	3A	
28	LVTTL-O	RxLOSDD	Loss of Signal for DD channel	3A	
29	LVTTL-I	Speed2DD	Tx Rate Select for DD channel	3A	
30		GND	Ground	1A	1
31		GND	Ground	1A	1
32	CML-O	RD1-	Inverse Received Data Out for DD channel	3A	
33	CML-O	RD1+	Received Data Out for DD channel	3A	
34		GND	Ground	1A	1
35		VccR1	Receiver Power for DD channel	2A	2
36		VccT1	Transmitter Power for DD channel	2A	2
37		GND	Ground	1A	1
38	CML-I	TD1+	Transmit Data In for DD channel	3A	
39	CML-I	TD1-	Inverse Transmit Data In for DD channel	3A	
40		GND	Ground	1A	1

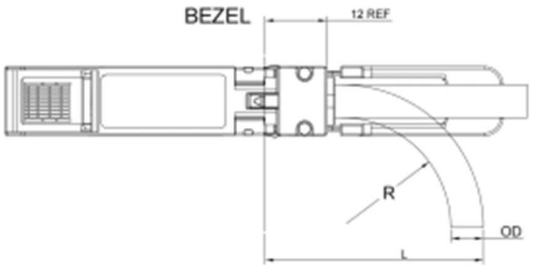
Notes:

1. SFP-DD uses common ground (GND) for all signals and supply (power). All are common within the SFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccR, VccT shall be applied concurrently and VccR1, VccT1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 12. VccR, VccT, VccR1, VccT1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. The ePPS pins (if not used) may be terminated with 50 Ω to ground on the host.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 0, 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 3 for pad locations) Contact sequence A will make, then break contact with additional SFP-DD/SFP-DD112 pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

Mechanical Dimensions







QSFP-DD				SFP-DD			
GAUGE	OD	BEND RADIUS "R"	MIN. BEND RADIUS "L"	GAUGE	OD	BEND RADIUS "R"	MIN. BEND RADIUS "L"
30AWG	12MM	60MM	126MM	30AWG	6MM	30MM	48MM
27AWG	14.4MM	72MM	150MM	27AWG	7.2MM	36MM	75MM

Ordering Information

Model Number	Description
QD-400G-SD-4X100G-005	400G QSFP-DD to 4xSFP-DD DAC, 30AWG, 0.5m, PVC, BLACK.
QD-400G-SD-4X100G-010	400G QSFP-DD to 4xSFP-DD DAC, 30AWG, 1.0m, PVC, BLACK.
QD-400G-SD-4X100G-015	400G QSFP-DD to 4xSFP-DD DAC, 30AWG, 1.5m, PVC, BLACK.
QD-400G-SD-4X100G-020	400G QSFP-DD to 4xSFP-DD DAC, 30AWG, 2.0m, PVC, BLACK.
QD-400G-SD-4X100G-025	400G QSFP-DD to 4xSFP-DD DAC, 27AWG, 2.5m, PVC, BLACK.
QD-400G-SD-4X100G-030	400G QSFP-DD to 4xSFP-DD DAC, 27AWG, 3.0m, PVC, BLACK.

References

1. QSFP-DD MSA Rev6.01
2. IEEE802.3cd
3. SFP-DD MSA